What is claimed is:

1. A flash memory comprising:

a memory cell array having pages, each of the pages including memory cells, bit lines and source lines;

a first circuit in signal communication with the bit lines for charging non-selected bit lines among the bit lines to a first voltage level at a first time;

a second circuit in signal communication with the bit lines for generating a pumping voltage higher than a power supply voltage at a second time; and

a third circuit in signal communication with the bit lines for charging the bit lines to a second voltage level at a third time.

2. The flash memory of claim 1, wherein the first voltage level is lower than the second voltage level.

3. The flash memory of claim 2, wherein the second voltage level is the power supply voltage.

4. The flash memory of claim 1, wherein the second time is longer than the first time by a predetermined interval.

5. The flash memory of claim 1, wherein the third time is longer than the second time by a predetermined interval.

6. The flash memory of claim 1, wherein the first circuit is responsive to a high voltage signal and address information associated with the non-selected bit lines, the high voltage signal being activated to generate the pumping voltage.

7. The flash memory of claim 1, wherein the first circuit is inactivated while an erase control signal is in an activated state.

8. The flash memory of claim 1, wherein the second circuit is inactivated while a predetermined pulse signal is in an activated state.

9. The flash memory of claim 8, wherein the pulse signal exists between the first time and the second time.

10. The flash memory of claim 1, wherein the third circuit charges the bit lines to the third voltage in response to a program start signal at the third time.

11. A flash memory comprising:

memory cell arrays having pages, each of the pages including memory cells, bit lines and source lines, the memory cell arrays being selectively driven according to address information;

a first circuit in signal communication with the bit lines for charging non-selected bit lines of the bit lines to a first voltage level at a first time;

a second circuit in signal communication with the bit lines for generating a pumping voltage higher than a power supply voltage at a second time; and

a third circuit in signal communication with the bit lines for charging the bit lines to a second voltage level at a third time, the bit lines being contained in selected memory cell array among the memory cell arrays.

12. The flash memory of claim 11, wherein the first voltage level is lower than the second voltage level.

13. The flash memory of claim 12, wherein the second voltage level is the power supply voltage.

14. The flash memory of claim 11, wherein the second time is longer than the first time by a predetermined interval.

15. The flash memory of claim 11, wherein the third time is longer than the second time by a predetermined interval.

16. The flash memory of claim 11, wherein the first circuit is responsive to a high voltage signal and the address information, the high voltage signal being activated to generate the pumping voltage.

17. The flash memory of claim 11, wherein the first circuit is inactivated while an erase control signal is in an activated state.

18. The flash memory of claim 11, wherein the second circuit is inactivated while a predetermined pulse signal is in an activated state.

19. The flash memory of claim 18, wherein the pulse signal exists between the first time and the second time.

20. The flash memory of claim 11, wherein the third circuit charges the bit lines to the third voltage in response to a program start signal at the third time, the bit lines being contained in the memory cell array selected according to the address information.

21. A flash memory comprising:

a first memory cell array for being selected when a predetermined address bit is in a first logic state;

first precharge transistors in signal communication with the first memory cell array for connecting bit lines of the first memory cell array to a power supply in response to a first precharge signal;

a second memory cell array disposed relative to the first memory cell array for being selected when the address bit is in a second logic state;

second precharge transistors in signal communication with the second memory cell array for connecting bit lines of the second memory cell array to the power supply in response to a second precharge signal;

a first circuit in signal communication with the bit lines of the first and second memory cell arrays for charging non-selected bit lines of the bit lines to a first voltage level at a first time;

a second circuit in signal communication with the bit lines of the first and second memory cell arrays for generating a pumping voltage higher than the power supply voltage at a second time; and

a third circuit in signal communication with the bit lines of the first and second memory cell arrays for charging the bit lines to a second voltage level at a third time, the bit lines being containing in a memory cell array selected according to the logic states of the address bit.

22. The flash memory of claim 21, wherein the first voltage level is lower than the second voltage level .

23. The flash memory of claim 22, wherein the second voltage level is the power supply voltage.

24. The flash memory of claim 21, wherein the second time is longer than the first time by a predetermined interval.

25. The flash memory of claim 21, wherein the third time is longer than the second time by a predetermined interval.

26. The flash memory of claim 21, wherein the first circuit is responsive to a high voltage signal and the address information, the high voltage signal being activated to generate the pumping voltage.

27. The flash memory of claim 21, wherein the first circuit is inactivated while an erase control signal is in an activated state.

28. The flash memory of claim 21, wherein the second circuit is inactivated while a predetermined pulse signal is in an activated state.

29. The flash memory of claim 28, wherein the pulse signal exists between the first time and the second time.

30. The flash memory of claim 21, wherein the third circuit activates one of main precharge signals according to the logic state of the address bit, the main precharge signals being responsive to a program start signal at the third time.